Flexibility Aware Systems-on-Polymer (SoP): Concept to Prototype

Ujjwal Gupta, Jaehyun Park, Hitesh Joshi and Umit Y. Ogras
School of Electrical, Computer, and Energy Engineering, Arizona State University
Email: {ujjwal, jpark244, hjoshi5, umit}@asu.edu

Abstract—Mechanically flexible, printed and stretchable electronics are gaining momentum. Rapid progress at device and circuit levels are already underway, but researchers are yet to envision the system design in a flexible form. This paper introduces *Systems-on-Polymer (SoP)* based on flexible hybrid electronics (FHE) to combine the advantages of flexible electronics and traditional silicon technology. First, we formally define flexibility as a new design metric in addition to existing power, performance, and area metrics. Then, we present a novel optimization approach to place rigid components onto a flexible substrate while minimizing the loss in flexibility. We show that the optimal placement leads to as much as 5.7× enhancement in flexibility compared to the naïve placement. We confirm the accuracy of our models and optimization framework using a finite element method (FEM) simulator. Finally, we demonstrate the SoP concept using a concrete hardware prototype and discuss the major challenges in the architecture and design of SoPs.

Index Terms—Flexible hybrid electronics, optimization, placement.

1 Introduction

Bendable, rollable, conformal, or elastic circuits, commonly known as flexible electronics, are emerging as a promising alternative to conventional rigid circuits. Systems designed using flexible electronics can be lighter, thinner and less expensive to manufacture [37]. Hence, they can enable wearable systems, such as electronic shirts, ties, and fire-fighter jackets, as well as arbitrarily shaped objects like electronic labels [18]. Current successful examples of flexible electronics include displays [5], sensors [46], photovoltaic cells [58], batteries [30], simple micro-controllers, radio frequency (RF) transmitters [1], and electronic paper [25].

Flexible electronics suffer severely from lower degrees of integration, limited performance and larger parameter variations compared to the state-of-the-art silicon technology, despite their huge potential in terms of new applications. For example, silicon technology offers 14nm feature size with an operating frequency in the order of 2GHz, while feature sizes of thin-film transistors (TFT) range from $8\mu\text{m}$ to $50\mu\text{m}$ [23], and frequencies hardly exceed a few MHz [29]. While this huge capacity gap can be reduced by novel approaches, such as carbon-based semiconductors [7, 50, 55], flexible electronics are still far from implementing a full-fledged multiprocessor systems-on-chip (SoC) with power and performance figures competitive with silicon technology. Consequently, practical use of flexible electronics is limited largely to sensors and displays [44, 45].

Emerging *flexible hybrid electronics* can target the short comings of flexible electronics by integrating traditional rigid chips and printed electronics on a flexible substrate [9, 43]. This hybrid approach combines the processing and storage capabilities of rigid chips with the physical and cost benefits of flexible electronics. We propose using FHE to implement electronic systems on flexible substrates, as depicted in Figure 1. Since the most common flexible substrates are plastic, polymer and paper, we coined the term SoP, which stands for *Systems-on-{Polymer, Plastic or Paper}* [21]. The idea behind this hybrid approach is to use rigid chips where high performance, processing and storage capabilities are needed, while reverting to flexible electronics for everything else to maintain the benefits of flexibility. By integrating flexible display, sensors, and battery with conventional chips, this generic architecture allows for a wide spectrum of systems ranging from simple internet-of-things (IoT) devices [32, 56] to complex mobile platforms like smart-phones [3]. Therefore, systems-on-polymer have the potential to transform personal computing by enabling arbitrary shaped wearable systems not limited to desks, laps or hands.

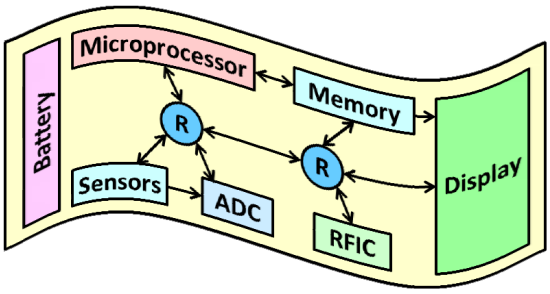


Fig. 1: A SoP with battery, sensors, ADC, microprocessor, memory, RFIC and display connected by flexible routers.

The fundamental difference between SoPs and SoCs is the physical flexibility. Larger number of rigid chips are

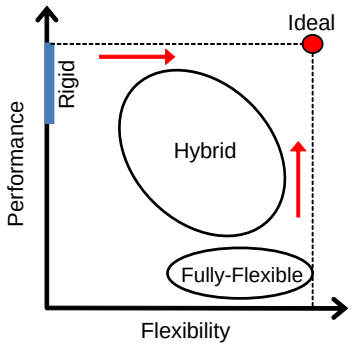


Fig. 2: Motivation for hybrid flexible electronics.

preferred to boost the processing power, since flexible electronics exhibit poor performance and scalability [25, 38]. However, using a large number of rigid chips would also undermine the advantages of flexibility. Furthermore, introducing flexibility inevitably introduces novel challenges, such as placement of rigid chips onto flexible substrates, and aggravates existing communication, reliability, power and thermal challenges. That is, FHE exhibit an inherent design trade-off between flexibility and computational efficiency (more rigid chips), as illustrated in Figure 2. Therefore, designing SoP architectures, such as the one illustrated in Figure 1, requires a formal and quantitative definition of flexibility as a new metric.

Besides introducing the SoP concept, this paper presents an analytical *flexibility* model as a new design metric in addition to traditional area, power, and performance metrics. Using this model, we construct an optimization approach to place rigid chips onto flexible substrates to maximize the flexibility. We show that the optimal placement leads to as much as 5.7× increase in flexibility compared to a naïve placement. We evaluate the accuracy of the analytical models and effectiveness of the proposed optimization approach using finite element method (FEM) simulations [51]. Finally, we demonstrate the SoP concept by presenting one of the first FHE prototypes implemented on a Polyimide substrate.

The major contributions of this paper are as follows:

- Defining flexibility as a new design metric for SoP architectures,
- A methodology for the optimal placement of rigid chips on a flexible substrate to maximize flexibility,
- A concrete SoP prototype for motion processing, and experimental evaluation of a printed antenna as a function of bending.

The rest of this paper is organized as follows. Section 2 overviews the related research. Section 3 presents the proposed flexibility model and optimal placement approach. Section 4 presents FEM simulation results that validate the proposed flexibility model, and discusses the optimization results. Section 5 presents a concrete SoP prototype and experimental results. Section 6 discusses the architectural challenges and potential research directions. Finally, Section 7 concludes the paper.

2 Related Research

Several institutions have recently demonstrated the feasibility of flexible electronics [1, 5, 20]. For example, flexible 8-bit MCU, ADC, and RFIC have been successfully manufactured using TowerJazz CS18 PD-SOI CMOS process. This hybrid approach to manufacturing flexible electronics uses lower CMOS technology nodes, then converts the circuit to flexible form-factor [1]. Fully flexible asynchronous MCU and SRAM have also been developed using low-temperature poly-silicon TFT technology [16, 28]. Similarly, integrated programmable logic circuits have been recently demonstrated in [47].

Prior research on electrical properties of fully flexible circuits—implemented using various technologies— has been demonstrated with the help of ring oscillators [12, 13, 27, 54, 57]. The work presented in [34] proposes a placement technique for TFTs by taking bending into account. In contrast, our approach is at macro-level, and targets FHE system design using rigid components on a flexible substrate. We refer the reader to [25] for a comprehensive overview of flexible electronics and associated design automation challenges.

Since flexible components have significantly lower performance compared to CMOS technology, using hybrid flexible electronics is encouraged by national research agencies [49]. Integration of CMOS devices on flexible substrates has recently been demonstrated at research centers including ASU Flexible Display Center [20, 48], industry [1] and academia [22]. However, only a handful of studies addressed the design of hybrid system design to date. Hu et al. [22] have recently presented a hybrid self-power system that combines sensing capabilities and long-range interconnects of large area flexible electronics with the processing advantages of CMOS chips. In [36], the authors present interface circuits between flexible electronics and CMOS chips using capacitively-coupled signals.

The early examples of FHE systems are critical milestones that show the feasibility of SoPs that can transform computer systems. However, the current technology mainly aims at individual devices [38]. Furthermore, there are no proposed solutions for the systematic design of flexible hybrid electronics systems. Towards developing a complete methodology, this paper takes a system level view and considers optimal integration of many macro-resources such as processor, display and sensors. We quantify flexibility as a new metric, and develop an optimal placement approach.

3 Optimum Placement of Rigid Components on Flexible Substrates

Physical flexibility is a new design dimension that has not been considered by computer system designers so far. In order to incorporate flexibility in the design process, we quantify the maximum deflection of a flexible substrate as a measure of flexibility. This formalism enables us to treat flexibility as a *measurable* design metric.

For example, it becomes possible to minimize the loss of flexibility under power/performance constraints, or impose a constraint on the loss in flexibility due to a rigid component. Then, we develop a design methodology for *optimally* placing rigid components on a flexible substrate with the objective of maximizing flexibility.

3.1 Flexibility Metric for Flexible Hybrid Systems

Consider a simple hybrid flexible system with one rigid component placed over a flexible substrate, as illustrated in Figure 3. We assume that the flexible substrate is a flat, homogenous isotropic material with uniform thickness. Figure 3 shows four pairs of uniformly distributed major bending forces that can be applied on the flexible substrate. All forces are normal to the plane of the flexible surface and uniformly distributed along the bending axis. We use the sum of the maximum deflection on each side of the rigid component as the flexibility metric, as described next.

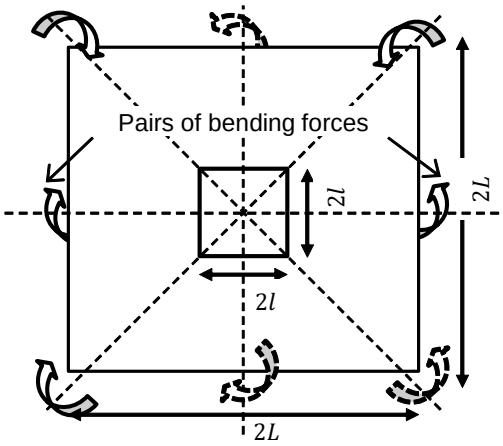


Fig. 3: A simple flexible hybrid system with one rigid component mounted over a large flexible substrate. Four possible uniform bending-force pairs are shown.

To analyze the impact of the relative size of a rigid component on flexibility, we consider a rigid chip of dimension $2l \times 2l$ mounted over flexible substrate of dimension $2L \times 2L$, as shown in Figure 3. We model this hybrid flexible system using two cantilever beams. First, the side-view of the flexible substrate alone and equivalent forces with pivot point are shown in Figure 4(a). Then, the corresponding view for the hybrid flexible system is repeated in Figure 4(b). We analyze the deflection at the sides as two separate cantilever beams when the rigid chip is placed at the center, as shown in Figure 4(c). In reality, the shear stress at the pivot will make some difference in the analysis of the pivoted beam and cantilever, but it is marginal and can be neglected due to thin flexible substrate. Cantilever beams with and without the rigid component are shown in Figures 4(d) and 4(e), respectively. These two figures illustrate that the rigid component decreases the effective length of the cantilever beam.

We can express the maximum deflection in a cantilever beam as a function of the uniformly distributed force P applied at one end (point force), modulus of elasticity E, and moment of area I: $\delta_{\max} = \frac{L^3 P}{3EI}$ [4]. Hence, the maximum deflection in the fully flexible (δ_{FF}), and hybrid flexible (δ_{HF}) systems shown in figures 4(d) and 4(e) are given by:

$$\delta_{FF} = \frac{L^3 P_{\max}}{3EI} \quad \text{and} \quad \delta_{HF} = \frac{(L-l)^3 P_{\max}}{3EI} \tag{1}$$

where $P_{\max}$ is the maximum force the substrate can sustain before breaking. If the contact (e.g., soldering) between the rigid component and flexible substrate is weaker than the flexible substrate, $P_{\max}$ will be smaller than actual material breaking force. We can compute the reduction in deflection using Equation 1 as:

$$\text{Deflection Loss} = \frac{\delta_{FF} - \delta_{HF}}{\delta_{FF}} = \frac{L^3 - (L-l)^3}{L^3} \tag{2}$$

Flexibility loss: The loss in flexibility is plotted in Figure 5 using Equation 2 as a function of the ratio between the lengths of rigid component and the flexible substrate. When the rigid component is 20% in length compared to the flexible portion, the flexibility loss is 45%. We observe that increasing the area of the rigid chip quickly diminishes the flexibility. Since moving more functionality to the rigid chips implies higher performance and larger rigid area, Equation 1 enables analyzing the tradeoff between the new flexibility metric and classical metrics such as area and performance.

So far, we have considered the scenario where the rigid chip is placed at the center for illustration purposes. If the rigid chip is placed at an arbitrary location x from one end point, as depicted in Figure 4(b), then the flexibility of hybrid flexible system can be found as:

$$\delta_{HF} = \frac{x^3 P_{\max}}{3EI} + \frac{(2L - 2l - x)^3 P_{\max}}{3EI} \tag{3}$$

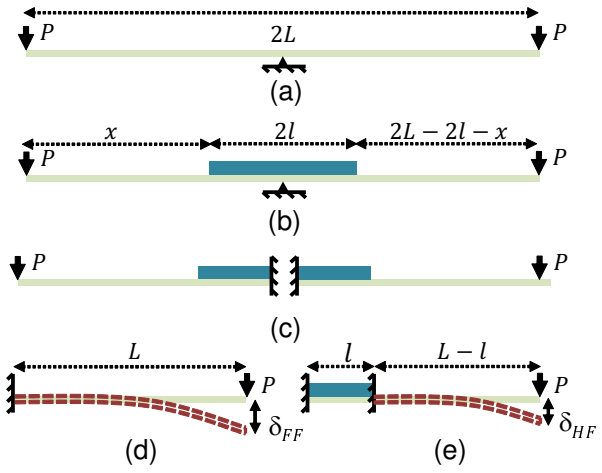


Fig. 4: Procedure for modelling the hybrid flexible system as a cantilever beam problem with special case, $x = L - l$.

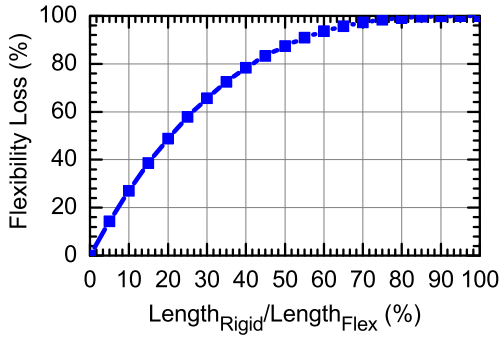


Fig. 5: The flexibility loss in hybrid flexible system compared to fully flexible system with one chip.

3.2 Flexibility Model with Multiple Rigid Chips

Suppose that N rigid chips need to be placed on a $H \times L$ substrate. Let h_i be the height, l_i be the length, and (x_i, y_i) be the lower left corner coordinate of the i^{th} chip. Any given pairs of chips should not overlap at least in one dimension to obtain a valid placement. For example, if two chips *do not* overlap along the x-axis, an overlap along the y-axis is allowed as illustrated in Figure 6. Therefore, we start off with placement along one dimension by considering the *non-overlapping* and *overlapping* scenarios separately.

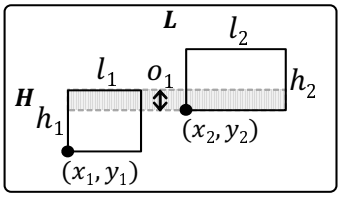


Fig. 6: A valid placement with overlap along y-axis.

Non-overlapping placement: Without loss of generality, assume that the rigid chips are ordered such that $x_i < x_j \implies i < j$. If the rigid chips are non-overlapping, the flexibility model given in Equation 3 can be extended to a function of N variables $\delta(\boldsymbol{x}) = \delta(x_1, x_2, \ldots, x_N) : \mathbb{R}^{\mathbb{N}} \rightarrow \mathbb{R}$ as:

$$\delta(\boldsymbol{x}) = \frac{P_{\max}}{3EI}\left[x_1^3 + \sum_{i=1}^{N-1}(x_{i+1} - (x_i + l_i))^3 + (L - (x_N + l_N))^3\right] \quad (4)$$

The first term inside the parenthesis (i.e., x_1^3) is the deflection due to the flexible region between the side $x = 0$ and the first rigid chip. Similarly, the last term gives the deflection due to the flexible region between the opposite side and the N^{th} chip. Finally, the intermediate terms represent the contributions due to the spacing between the rest of the rigid chips.

Overlapping placement: If the rigid chips can overlap, we also need to account for the overlap to extend the flexibility model. In this case, we assume $\min_{1 \le i \le N} x_i = x_1$, i.e., the index of the rigid chip with the smallest $x-$coordinate is 1. The rest of the chips are ordered such that $(x_i + l_i) \le (x_j + l_j) \implies i < j$. That is, the ordering is with respect to the $x-$coordinate of the right side. Let o_i $1 \le i < N$ be the overlap between the i^{th} and $(i+1)^{\text{th}}$ rigid chip. Note that $0 \le o_i \le min(l_i, l_{i+1})$, $1 \le i < N$. That is, the overlap between any pair of chips cannot exceed the length of the shorter one. Using this definition, we introduce the following change of variable to expresses the $x-$coordinate of the rigid chips: $x_{i+1} = x_i + l_i - o_i$, $1 < i < N$. This enables us to express the coordinates as:

$$\begin{aligned} x_2 &= x_1 + l_1 - o_1 \\ x_3 &= x_2 + l_2 - o_2 = x_1 + (l_1 + l_2) - (o_1 + o_2) \\ \ldots &\quad \ldots \\ x_N &= x_1 + \sum_{i=1}^{N-1} l_i - \sum_{i=1}^{N-1} o_i \end{aligned} \quad (5)$$

Using these expressions, the flexibility model for N rigid chips that can overlap can be written as a function of N variables $\delta(x_1, \boldsymbol{o}) = \delta(x_1, o_1, o_2, \ldots, o_{N-1}) : \mathbb{R}^{\mathbb{N}} \rightarrow \mathbb{R}$,

$$\delta(x_1, \boldsymbol{o}) = \frac{P_{\max}}{3EI}\left[x_1^3 + \left(L - \left(x_1 + \sum_{i=1}^{N} l_i - \sum_{i=1}^{N-1} o_i\right)\right)^3\right] \quad (6)$$

Similar to the non-overlapping case, the first term inside the parenthesis is the deflection due to the flexible region between the side $x = 0$ and the first rigid chip, while the last term gives the deflection due to the flexible region between the opposite side and the N^{th} chip. The intermediate terms vanish, since the rigid chips have non-zero overlap.

3.3 Optimal Placement along One Dimension

In this section, we present a theorem that specifies the optimal placement along $x-$dimension using Equation 4 and Equation 6. We will use this result to develop a methodology to place multiple rigid chips on a 2D substrate to maximize the flexibility.

Theorem 1: Consider the placement of N rigid chips along one dimension (e.g., x-axis as shown in Figure 4).

1) *If the rigid chips are* ***not allowed to overlap****,* the flexibility is maximized when all the chips are placed side by side (i.e., they form a contiguous region), at either side of the substrate, as illustrated in Figure 7(a). The maximum flexibility in this case is given as,

$$\delta_{\text{nonoverlapping}} = \frac{P_{\max}}{3EI}\left(L - \sum_{i=1}^{N} l_i\right)^3 \quad (7)$$

2) *If the rigid chips* ***can overlap****,* the flexibility is maximized if the chips are placed at either side, and the overlap between each pair is *maximum*, as illustrated in Figure 7(b).
The maximum flexibility in this case is given as,

$$\delta_{\text{overlapping}} = \frac{P_{\max}}{3EI}\left(L - \max_{1 \le i \le N} l_i\right)^3 \quad (8)$$

The proof of this theorem is presented in the Appendix.

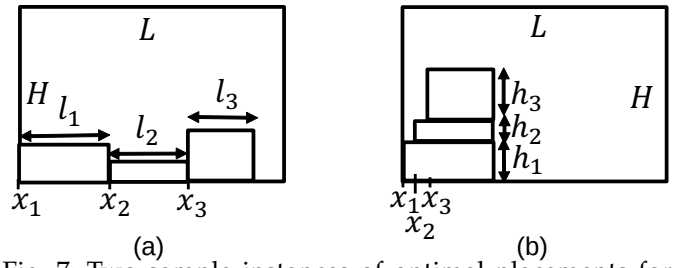


Fig. 7: Two sample instances of optimal placements for (a) non-overlapping and (b) overlapping in x-dimension.

3.4 Optimal Placement on a Flexible 2D Substrate

An important optimization criterion for 2D placement is the bending axis. For instance, horizontal bending is the primary concern in a wearable device in the form of a wristband. In general, horizontal, vertical, or diagonal bending, or even a combination might be of interest depending on the target application. Given the optimization goal, the theorem presented in Section 3.3 can be utilized within an algorithm to place multiple rigid chips on a 2D flexible substrate. The simplest solution would be an iterative heuristic that can place the rigid chips one by one so as to maximize the flexibility criterion at each step. More precisely, it can first place the next rigid component to form a contiguous region with *no-overlap* along $x-$axis and *overlap* along $y-$axis. Then, it can compare this solution to the placement with *overlap* along $x-$axis and *no-overlap* along $y-$axis. In this way, multiple chips can be sorted and placed iteratively. A better approach would employ a more thorough backtracking algorithm, such as a depth first search [52], to perform a global search. However, the combinatorial nature of an exhaustive search can quickly explode the complexity, when the number of rigid chips and bending scenarios increase. Therefore, we propose the approach described next.

In general, Theorem 1 indicates that the rigid chips should be packed to form a contiguous region, and placed at the side of the substrate which is parallel to the bending axis. Since packing the chips densely also reduces the interconnect length, we propose first packing the rigid chips into the smallest bounding-box *with a soft aspect ratio* using existing floorplanning techniques [2, 17]. Then, we define the bounding-box as the rigid area, as shown in Figure 8. Our objective is to find the *optimal placement*, *aspect ratio* and *orientation* of the bounding-box as a function of the bending axis.

The geometric representation of a generic problem instance is shown in Figure 8. Consider a flexible substrate $ABCD$, with the coordinates $A(0,0)$, $B(L,0)$, $C(L,H)$ and $D(0,H)$, respectively. The bounding-box $pqrs$ is placed with an arbitrary orientation angle θ with respect to the horizontal side of flexible substrate. The area of the bounding-box B_A is fixed, while the length l and height h are free variables where $B_A = l \times h$. Let the coordinates of point r be (x_r, y_r), then the coordinates of points s, p and q can be written as:

$$(x_s, y_s) \equiv (x_r + hcos\theta, y_r + hsin\theta), \quad (9)$$

$$(x_p, y_p) \equiv (x_r + dcos(\theta + \phi), y_r + dsin(\theta + \phi)), \quad (10)$$

$$(x_q, y_q) \equiv (x_r + lcos(\theta + \pi/2), y_r + lsin(\theta + \pi/2)), \quad (11)$$

where $\phi = tan^{-1}(l/h)$ and $d = \sqrt{l^2 + h^2}$.

The flexible substrate can be bent across an arbitrary bending axis such as a_1 and a_2 shown in Figure 8. For example, when the bending angle β (the angle between a_2 and x-axis) is zero, the substrate is bent horizontally, i.e., along the x-axis. Likewise, $\beta = \pi/2$ implies vertical bending along the y-axis. We consider uniform bending all throughout the flexible substrate, and model the system using cantilever beams. Since maximum deflection is proportional to the cube of length (Equation 1), the longest cantilever beam will give the largest deflection for a given amount of force applied. For example, consider the two cantilever beam models, $|\mathrm{Am}|$ and $|\mathrm{Cn}|$ shown in Figure 8. These cantilever beams are perpendicular to the two axes a_1 and a_2 and represent the longest length out of all other possible cantilevers. $|\mathrm{Am}|$ and $|\mathrm{Cn}|$ can be found as:

$$|\mathrm{Am}| = x_r sin\beta + y_r cos\beta \quad (12)$$

$$|\mathrm{Cn}| = (L - x_r - dcos(\theta + \phi))sin\beta + (L - y_r - dsin(\theta + \phi))cos\beta \quad (13)$$

In general, the flexibility can be written as sum of deflections of these two cantilever beams as follows:

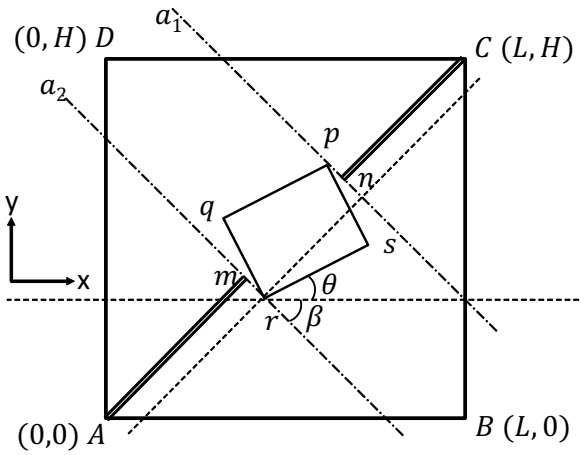


Fig. 8: Geometric illustration of an arbitrary bounding-box $pqrs$ with orientation θ over a flexible substrate $ABCD$ is shown. The bending axes a_1 and a_2 are parallel and equivalent to any other bending axis at an angle β and not intersecting the bounding-box region. $|\mathrm{Am}|$ and $|\mathrm{Cn}|$ are the lengths of cantilever beams.

$$\delta(x_r, y_r, \theta, \beta, l, h) = \frac{P_{max}}{3EI}\Big[(x_r sin\beta + y_r cos\beta)^3 + ((L - x_r - dcos(\theta+\phi))sin\beta + (L - y_r - dsin(\theta+\phi))cos\beta)^3\Big] \quad (14)$$

Equation 14 gives the flexibility for an arbitrary bending axis with angle β. Therefore, we can find the optimum dimensions l and h, orientation θ, and location (x_r, y_r) for the rigid bounding-box as a function of β. Depending on the usage scenario, we may want to bend the flexible substrate along multiple axes. For example, one might co-optimize for both horizontal and vertical bending instead of considering only one of them. Therefore, we define a set of bending angles, $\boldsymbol{\beta} = [\beta_1, \beta_2, \beta_3 ..., \beta_n]$ with respective relative importance $\boldsymbol{W} = [w_1, w_2, w_3, ...w_n]$. As a result, we can define the objective function as a weighted sum of flexibility at different bending angles:

$$\Delta(x_r, y_r, \theta, l, h, \boldsymbol{\beta}, \boldsymbol{W}) = \sum_{i=1}^{N} w_i \times \delta_i(x_r, y_r, \theta, \beta_i, l, h) \quad (15)$$

Our goal is to maximize the flexibility under the geometric constraints. This can be expressed using a nonlinear optimization problem as follows:

$$\begin{aligned} \text{maximize} \quad & \Delta(x_r, y_r, \theta, l, h, \boldsymbol{\beta}, \boldsymbol{W}) \\ \text{subject to} \quad & g_c : 0 \le x_p, x_q, x_r, x_s \le L, 0 \le y_p, y_q, y_r, y_s \le H, \\ & g_\beta : 0 \le \boldsymbol{\beta} \le \boldsymbol{\pi/2}, \\ & g_\theta : -\min(\boldsymbol{\beta}) \le \theta \le -\max(\boldsymbol{\beta}) + \pi/2, \\ & g_l : l \ge L_{\min}, \;\; g_h : h \ge H_{\min} \\ & \text{Area of bounding-box} : B_A = l \times h, \\ & \sum_{i=1}^{N} w_i = 1, \;\; w_i \ge 0 \;\forall i \end{aligned} \quad (16)$$

The first inequality ensure that the bounding-box $pqrs$ remains within the flexible substrate boundary, while the second one constrains the bending angle g_β to the interval $[0, \pi/2]$. Similarly, g_θ constrains θ w.r.t. the maximum and minimum β values. The constraints g_β and g_θ avoid symmetric solutions. We also have constraints for the area B_A, minimum length g_l, and minimum height g_h of the bounding-box. Finally, weight of all bending angles sum to one, and all quantities except θ remain positive throughout the optimization.

System designers may want to pre-specify flexible only regions on the substrate where no rigid chips can be placed. For example, consider an arbitrary shaped flexible-only region R_{FF} as an input to the optimization framework. The bounding-box region R_{BB} should be placed such that it does not intersect the flexible region R_{FF}, *i.e.*, $R_{FF} \cap R_{BB} = \phi$. The separation between the two regions can be achieved by adding more constraints to the optimization formulation given in Equation 16. In particular, Linear Discriminant Analysis [6] can be used to check for the condition of existence of an affine transformation $f(x, y) = \mathbf{a}^T \begin{bmatrix} x \\ y \end{bmatrix} - b : \mathbb{R}^2 \to \mathbb{R}$ between the two regions.

$$\mathbf{a}^T \mathbf{p_R} - b \ge t, \quad \mathbf{p_R} \in R_{FF} \quad (17)$$

$$\mathbf{a}^T \mathbf{q_R} - b \le -t, \quad \mathbf{q_R} \in R_{BB} \quad (18)$$

where t is the margin between the affine transformation and the two regions R_{FF} and R_{BB}. If $\mathbf{a}$ and b exist for a given R_{FF} and R_{BB} then the regions do not overlap and the bounding-box placement is valid. Therefore, with these constraints, the placement approach can avoid certain pre-defined regions.

4 FEM Validation and Optimization Results

In this section, we first present FEM simulation results to validate the accuracy of our flexibility metric. Then, we discuss optimization results obtained by solving the nonlinear program given in Equation 16.

4.1 Flexibility Model Validation

Simulation is an important component of electronic system design flows, since it provides a trade-off between accuracy and speed. In our context, we have to validate the accuracy of the second order flexibility model given in Equation 1, before employing it for optimization. This validation can serve as a strong basis for FHE optimization approaches, such as our placement technique, that utilize the proposed flexibility model. We employ COMSOL [10] multi-physics software to perform FEM simulations, since it enables realistic study of multiple physical phenomena, such as electrical inputs and structural deformations.

As the first step to validate the proposed flexibility model, we built the substrate and bounding-box geometry shown in Figure 4(e). We chose a Polyimide substrate, since it is widely used in industry [14]. The output of FEM simulations and the analytical solution from Equation 1 are plotted in Figure 9. The average percentage error between our analysis and FEM simulations is 2.0%. Moreover, the deflection of the SoP

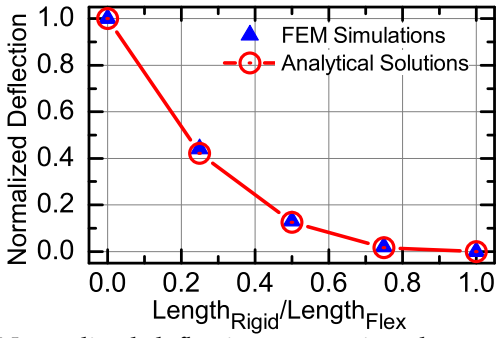


Fig. 9: Normalized deflection comparison between FEM simulations and analytical model given in Equation 3.

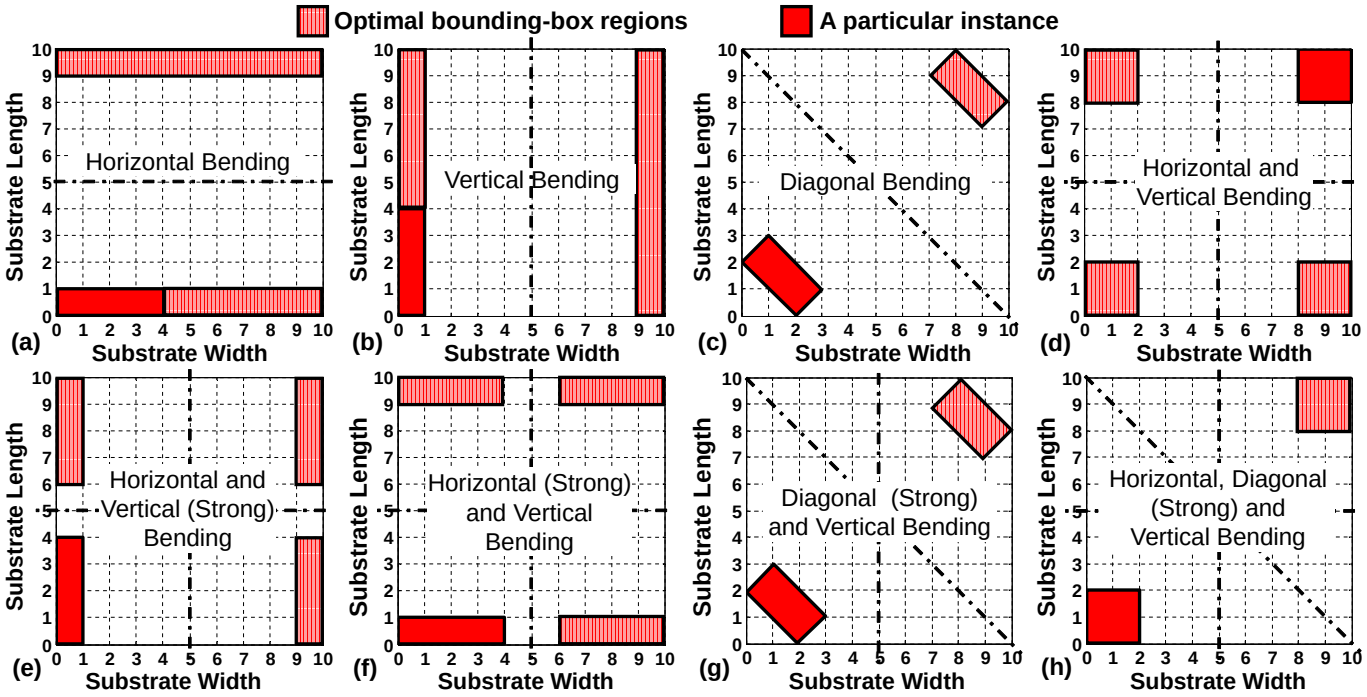


Fig. 10: Optimal bounding-box regions for the flexible hybrid system.

decreases with increasing size of the rigid bounding-box, as expected. In summary, the validation results show that our deflection model is highly representative of the real behavior. Therefore, it can be employed by other researchers to develop FHE optimization techniques. Furthermore, this simulation setup enables us modeling a large set of real-life scenarios.

4.2 Optimization Results

We solved the general optimization problem given by Equation 16 using numerical techniques in Matlab for 10 units $\times$ 10 units flexible substrate and a bounding-box with area $B_A = 4$ units^2. We also derived the analytical solution for special cases $\beta = 0$ and $\beta = \pi/2$ for validation purposes. Since the most common bending angles are horizontal, vertical and along the diagonal, we set $\boldsymbol{\beta} = [0, \pi/4, \pi/2]$ to analyze the optimal placements.

Figure 10(a) shows the optimal placement under horizontal bending ($\boldsymbol{W} = [1, 0, 0]$). The optimal orientation is $\theta = 0$, while the dimension of bounding-box is 4×1. This implies that the height of the optimal bounding-box comes out to be equal to the constraint, $H_{\min} = 1$. That is, the orientation is parallel to the bending axis and the dimension perpendicular to the bending axis is minimized as expected. Furthermore, we observe that the bounding-box can be placed at either side. This makes sense since the maximum displacement depends on the cube of the distance from the side, which is maximized when the bounding-box touches at either side. Similarly, for vertical bending ($\boldsymbol{W} = [0, 0, 1]$), the optimal orientation is $\theta = -\pi/2$, dimension of bounding-box is 4×1, and the placement is either at $x_r = 0$ or $x_r = 9$, as shown in Figure 10(b). When the bending is along the diagonal ($\boldsymbol{W} = [0, 1, 0]$), as shown in Figure 10(c), the orientation is $\theta = \pi/4$, as expected. We also note that the optimal dimensions are 1.41×2.83, which is non-trivial unlike the previous cases, while the placement was at either corner.

More complex scenarios with multiple bending angles are shown in Figures 10(d)–10(h). For vertical and horizontal bending together ($\boldsymbol{W} = [0.5, 0, 0.5]$), the output is $\theta = 0$, dimension of bounding-box is 2×2, and possible locations are $(0, 0), (0, 8), (8, 0)$, and $(8, 8)$, as shown in Figure 10(d). Note that, the result is same irrespective of any amount of additional diagonal bending as shown in Figure 10(h). The results with $\boldsymbol{W} = [0.25, 0, 0.75]$ and $\boldsymbol{W} = [0.75, 0, 0.25]$, shown in Figures 10(e) and 10(f) are similar to Figures 10(b) and 10(a), respectively. However, only the corners are optimal. For strong diagonal and vertical bending ($\boldsymbol{W} = [0, 0.75, 0.25]$), the result is similar to Figure 10(c), but has slightly different dimensions of bounding-box (1.46×2.73) and possible location $(0, 1.93)$. The tendency is to move the bounding-box towards the corners of the flexible substrate.

A naïve approach to place the bounding-box on the substrate could be at the center with dimensions 2×2, similar to the placement in Figure 3. The flexibility comparison of naïve approach versus the result of the optimized placement is shown in Table 1. The optimal solution gives $4.58\times$ gain in flexibility on average. These results show substantial improvements in flexibility and signify the importance of optimal placement for wearable computing system design.

TABLE 1: The gains in flexibility are shown by placing the bounding-box optimally (Δ^*) as opposed to naïve placing it at the center (Δ_{center}) of the substrate with dimensions $10\text{cm} \times 10\text{cm} \times 300\mu\text{m}$, Elasticity $E = 7.95\text{GPa}$, and an applied force of 100N/m^2.

Figure 10 index	Weight Vector			Max. Deflection (mm)		Gain in Flexibility
	W_0	$W_{\pi/4}$	$W_{\pi/2}$	Δ_{center}	Δ^*	
(a)	1.00	0.00	0.00	0.06	0.35	5.69 ×
(b)	0.00	0.00	1.00	0.06	0.35	5.69 ×
(c)	0.00	1.00	0.00	0.25	0.99	4.00 ×
(d)	0.50	0.00	0.50	0.06	0.25	4.00 ×
(e)	0.25	0.00	0.75	0.06	0.29	4.69 ×
(f)	0.75	0.00	0.25	0.06	0.29	4.69 ×
(g)	0.00	0.75	0.25	0.20	0.79	3.91 ×
(h)	0.20	0.60	0.20	0.17	0.69	4.00 ×

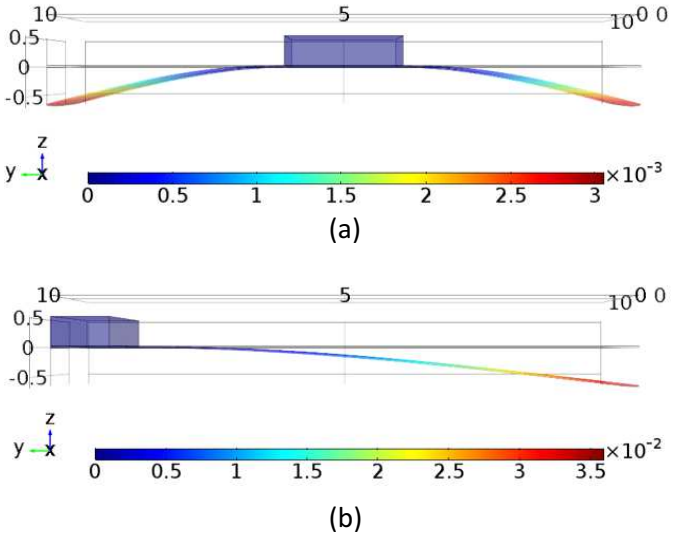


Fig. 11: The cross-sectional view of the COMSOL model when the bounding-box is at the (a) center and (b) side.

4.3 Validation of the Optimization Results

Once the accuracy of the flexibility model is established, we performed FEM simulations to validate the proposed optimum placement approach. To achieve this, we simulated all the bending scenarios considered in Figure 10, and placing the substrate to the center of the substrate. For example, Figure 11(a) and (b) show the cases when the bounding-box is at the center and at the left hand side of the substrate, respectively. In agreement with the analytical results, placing the bounding-box to the side delivered $5.81\times$ improvement in flexibility over placing it to the center. Figure 12 compares the FEM simulation results and analytical solutions for each of the bending scenario shown in Figure 10. We observe that the analytical model exhibits a high fidelity across all the scenarios with horizontal and vertical bending. More precisely, the mean absolute percentage error between the flexibility of analytical and FEM simulation results is 5.9%.

5 System on Polymer Prototype

To demonstrate the feasibility of SoP architectures, we designed and manufactured a hardware prototype as

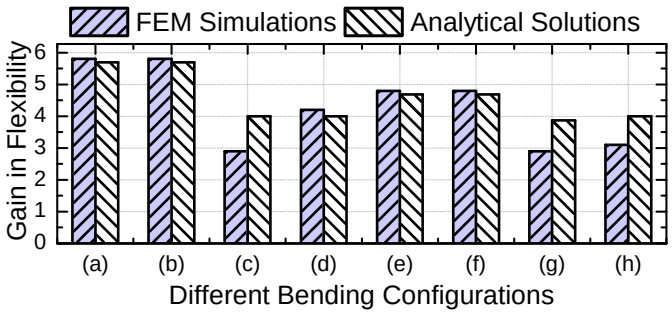
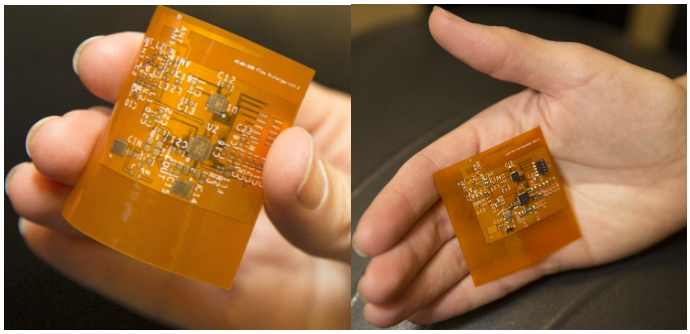


Fig. 12: Gain in flexibility for different bending axis presented in Figure 10. (a), (b), (c), (d), (e), (f), (g), (h) corresponds to various bending configurations in Figure 10.

an early proof of concept. We envision that FHE will be commonly used for designing wearable IoT devices. Therefore, our prototype integrates sensing, processing and wireless communication in a form factor that can fit into the palm. We chose motion tracking and processing as the driver application, since it can be used in a wide range of applications from fitness tracking to gesture recognition. The prototype can be attached to the sleeve of clothing or placed into the palm, as illustrated in Figure 13.

The complete list of the resources used in the prototype is provided in Table 2. The flexible Polyimide substrate used in our prototype has several advantages compared to a rigid FR-4 substrate. For example, the flexible substrate is lighter, thinner, and can enable integration into wearable systems, such as electronics shirts, wrist bands, and electronic labels. To implement our driver application, we used a Motion Processing Unit (MPU) [26] that integrates accelerometer and gyroscope sensors built on MEMS technology. We employed a rigid MPU in our prototype mainly due to its size advantages. In general, sensing is one of the most promising subsystem that can be fully flexible. We are planning to use flexible photo-voltaic cells to our next generation prototype to add solar charging capability. The sensor data from the MPU is first digitized using an analog to digital convertor. Then, it is transmitted to a TI CC2650 microcontroller (MCU) [53] via serial interface, such as



(a) Unmounted flexible bare-board. (b) The prototype with all the chips mounted.

Fig. 13: The SoP prototype as bare board and with components mounted.

TABLE 2: Summary of area of different components in the SoP prototype.

Type	Components	Total no of components	Total area (mm^2)
Rigid	Microcontroller (CC2650F128RSM)	1	16
	Motion Processing Unit (MPU9250)	1	9
	Oscillator1 (32.768 KHz)	1	4.8
	Oscillator2 (24 MHz)	1	8
	Voltage regulator	1	7.5
	Passive elements	41	3.48
Semi-Flexible	Copper plane + Antenna	1	1332.51
Flexible	Polyimide substrate	1	2500
Debug circuits	JTAG header	1	45.72
	Power test points	2	26.98

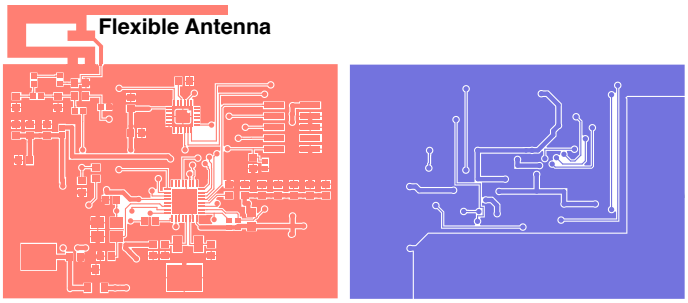
I2C and SPI [33]. In general, powerful rigid chips are best suited to satisfy the performance requirements of processing tasks like gesture generation in a small footprint. However, flexible MCUs have also started to emerge as an alternative [1], albeit with lower computational capabilities. Our prototype transmits the processed data wirelessly to a smartphone using a Bluetooth Low Energy interface [19] and a flexible inverted-F antenna. The flexible inverted-F antenna enables data transmission with the same performance as a rigid antenna, as will be shown in Section 5.2. If we had used a rigid antenna, the flexibility of the SoP prototype would have decreased. Therefore, a flexible antenna is a better choice that gives same performance, but more flexibility compared to a rigid antenna. Finally, we interpreted and visualized the motion using a custom application running on the phone.

We performed extensive FEM simulations to evaluate different placement options for our prototype. In particular, we report simulation results for three scenarios:

1) The rigid chips are packed as dense as possible into a bounding-box. Then, the bounding-box is placed at one of the corners. This corresponds to the solution recommended by the proposed placement algorithm, which is also adapted in the current prototype,
2) The bounding-box is placed to the center of the substrate. This scenario enables quantitative comparison of the flexibility gain to the analytical results reported in Table 1,
3) The rigid chips are placed sparsely to facilitate wire routing rather than placement.

The recommended placement leads to $2.1\times$ gain in flexibility compared to placing the bounding-box to the center, which is aligned with the analytical results. Furthermore, the optimal solution gives $4.2\times$ better flexibility than the sparse placement. This result validates our choice of packing the rigid chips as dense as possible. In summary, FEM simulations confirm the optimality of placing the smallest possible bounding-box at a corner, which is a direct result of our placement methodology.

The optimized PCB layouts of the top and bottom layers of the bounding-box in the prototype are shown in Figure 14(a) and Figure 14(b), respectively. We emphasize that the JTAG interface and debugging circuity are added to facilitate debugging and programming. Therefore, the size of a product version of this prototype can be reduced by more than 50%.



(a) Top layer. (b) Bottom layer.

Fig. 14: SoP prototype top and bottom layouts.

5.1 SoP Prototype Characteristics

The characteristics of the prototype are summarized in Table 3. The prototype can transmit up to 192kbps to the host computer, but we set the sampling period as 100ms to minimize the energy consumption. This makes the transmission throughput as 1.44kbps. The power consumption is measured using Monsoon power meter [35] as 12.21mW, which leads to 9.54μJ energy consumption to send one bit. The runtime power statistics of the SoP prototype according to the operating mode are summarized in Table 4. The experimental prototype is powered through an external source. However, we plan to use flexible batteries mounted on the bottom layer of the SoP. We expect about 40 hour lifetime under continuous use, when we employ a 130mAh flexible battery [41].

TABLE 3: Characteristics of the SoP prototype.

Maximum performance	Operating performance	Connection interval	Energy/Tx
192kbps	1.44kbps	100ms	9.54μJ/bit

5.2 Flexible Antenna Experiments

It has been shown that the return loss of flexible antennas, such as a bow-tie antenna, may increase with

TABLE 4: Average power measurement summary during different operating modes of the SoP prototype.

Power consumption	Idle	Advertising	Connected idle	Tx sensor data
Peak (mW)	–	30.17	–	29.73
Average (mW)	3.59	4.27	3.60	12.21

bending [15]. To minimize the impact of bending, we employed an omnidirectional 2.4GHz inverted-F antenna on our FHE prototype, as shown in Figure 13(a). To evaluate the antenna properties under different bending scenarios, we performed experiments inside a Faraday cage, as depicted in Figure 15.

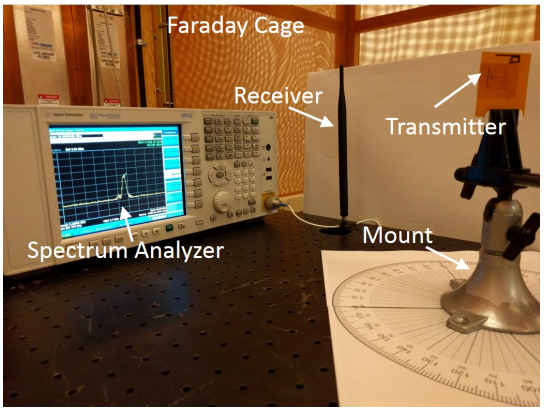


Fig. 15: Experimental setup for antenna measurements.

First, we confirmed that the center frequency of the antenna remains constant irrespective of bending. This is expected, since bending does not affect the antenna dimensions. Then, we analyzed the received signal power as a function of bending, when the receiver was 1m away from the transmitter. In particular, we measured the received signal power when the prototype was flat and bent along 1.5cm and 2cm radii of curvature. We also repeated the measurement for inwards and outwards bending, as illustrated in Figure 16(a) and Figure 17(a). Figure 16(b) shows that the received power is affected significantly by inwards bending. For example, the received power decreases by as much as 5dB, when the angle (θ) between the transmitter and receiver varies from 0° to 180°. This is roughly equivalent to increasing the separation between the transmitter and receiver by 2.5×. At the same time, the received signal power increases at certain angles, such as 60°. We conclude that the change in the received power stems primarily from multiple scattering due to electronic components on the interior side of the prototype. As a result, mostly destructive but also occasional constructive interference occurs at the receiving monopole antenna. This conclusion is supported by the results obtained for *outward* bending, as shown in Figure 17(b). Outward bending causes significantly smaller interference, and leads to significantly smaller variation due to bending. Figure 17(b) also clearly demonstrates the omni-directional nature of the inverted-F patch antenna. In summary, this study shows that (1) bending may have intricate implications despite designing the antenna carefully, (2) inverted-F antenna can be a promising solution for flexible systems.

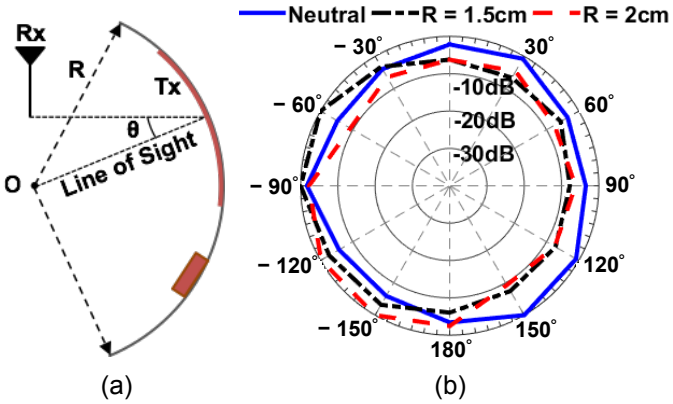


Fig. 16: (a) Illustration of inward bending. (b) Normalized radiation patterns of the flat and inward bent board.

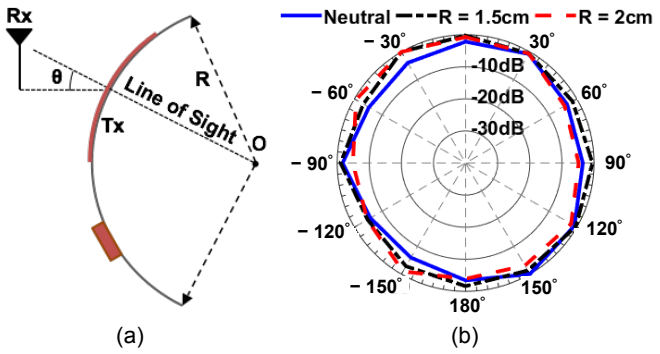


Fig. 17: (a) Illustration of outward bending. (b) Normalized radiation patterns of the flat and outward bent board.

6 FHE Design Challenges and Future Research Directions

Next, we overview major challenges in the design of SoP architectures, and discuss potential research directions.

SoP Communication Challenges: A flexible circuit can be bent into several millimeter radius before strain-induce damage to circuits. Bending the substrate can change the electron mobility by as much as 20%, and affect the timing of flexible circuits [42]. Moreover, physical changes in the substrate affect the interconnect capacitance, leading to further timing uncertainties. To analyze the effect of bending on flexible circuits, we first designed Pseudo-E CMOS type [24] inverter using IGZO TFT technology [39], as shown in Figure 18(a). We chose Pseudo-E CMOS inverters, since IGZO TFT technology supports only n-type transistors. Then, we implemented a ring oscillator given in Figure 18(b) using the Pseudo-E CMOS inverters. SPICE simulations

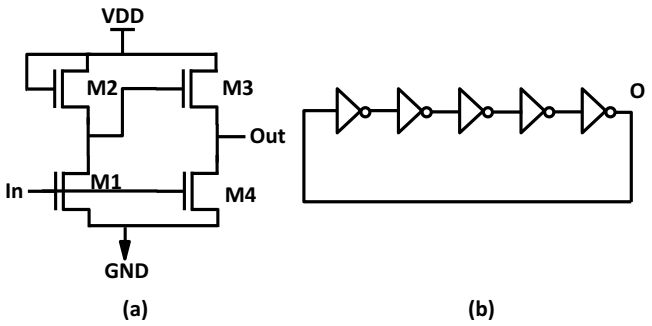


Fig. 18: (a) Design of basic pseudo-E CMOS inverter [24]. The W/L ratio used in this paper for M3 is $9\mu m/9\mu m$ and for all other transistors is $18\mu m/9\mu m$. (b) The circuit diagram of a ring oscillator made using pseudo-E CMOS inverters.

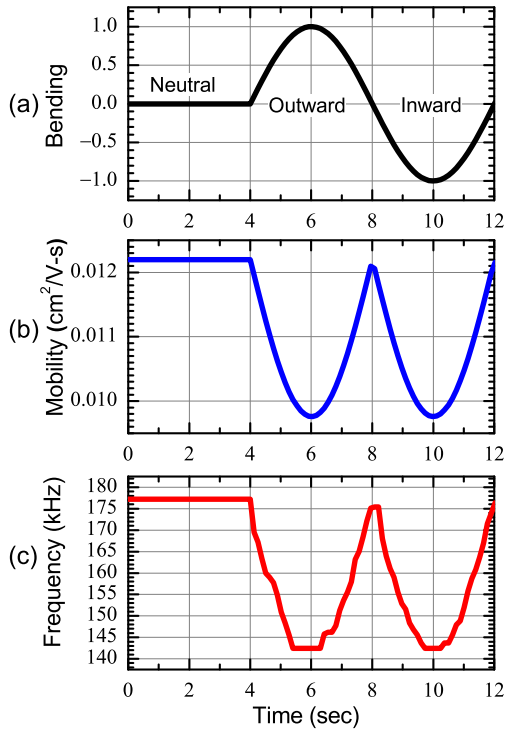


Fig. 19: The change in ring oscillator frequency because of change in mobility due to bending.

showed a nominal operating frequency of 175kHz for this circuit. Then, we emulated the bending scenario described in Figure 19(a) by modulating the mobility. Initially, the mobility remained constant (labeled as Neutral in Figure 19(a)). Next, the mobility decreased following a sine wave pattern to emulate outward and inward bending consecutively, as illustrated in Figure 19(b). As the mobility varied, we analyzed the output frequency of the ring oscillator. Figure 19(c) shows the variation in the ring oscillator frequency with bending. When there is no bending (Neutral position), the ring oscillator was measured as 175kHz. As the circuit was bent, the carrier mobility decreased, leading to longer inverter propagation delay. The longer delay, in turn, decreased the ring oscillator frequency, as illustrated in Figure 19(c). In particular, the lowest frequency, observed at the maximum bending point, was recorded as 142kHz.

We also performed Monte Carlo simulations to validate our bending approximation by varying mobility in a Gaussian fashion. We found that the variation in frequency generated by the ring oscillator is between 150kHz to 175kHz, as shown in Figure 20. This frequency range is well within the bounds of frequency shown in Figure 19.

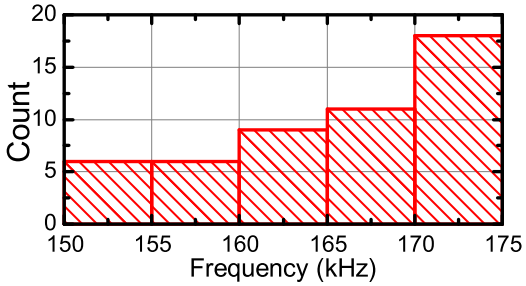


Fig. 20: Frequency histogram obtained by Monte Carlo simulation of the ring oscillator for 20% change in mobility.

Since the bending axis and amount of bending cannot be known a priori, the changes in timing and clock period of printed circuits are unpredictable. Consider the circuit in Figure 21, which shows a combinational path between two registers. Bending can lead to setup and hold time violations as a function of the changes both in the delay of clock and combinational path. Designing for the worst case would deteriorate the performance, which is already suffering from low speeds and large feature sizes compared to silicon chip. Furthermore, techniques proposed to improve the reliability by dynamically detecting timing violations have also limited applicability since they would be also affected by bending. For example, we implemented the slack-probe technique [31] using TFTs to cope with timing variations. Our simulations showed that the circuit can hardly reach 500Hz.

Timing and synchronization in flexible circuits are complicated by factors including supply-voltage, thermal, parameter variations, and bending. Therefore, asynchronous, or globally asynchronous locally synchronous (GALS) [40] communication, and latency insensitive design techniques [8, 11] are much better fit for SoP communication. GALS is particularly attractive since different synchronous rigid chips can communicate over a network composed of asynchronous routers [40].

Potential Research Directions: There are a number of interesting research directions related to FHE. Manufacturing solutions and I/O interfaces, especially for stretchable electronics, will be a major driver for practical FHE solutions. Related to this, reliability is a major concern at both the material and system level, since FHE systems are subject to continuous physical deformation.

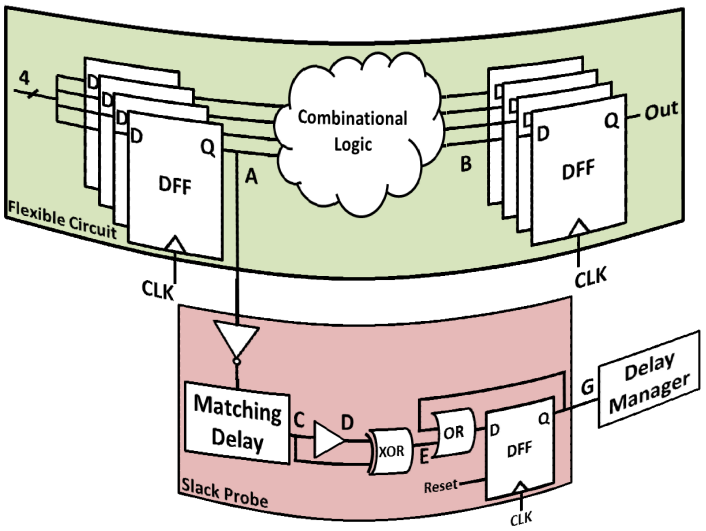


Fig. 21: Flexible circuit pipeline showing four input and four output registers with combinational logic. A slack-probe [31] has been inserted at point A, to detect delay failure.

For example, the drain current of the ultraflexible pentacene FETs changes by about 10% after 160,000 bending cycles [42]. Since neither active cooling nor large heat sinks can be used on flexible substrates, novel thermal and power management techniques targeting SoPs are needed. Finally, security and privacy will be important considerations, as FHE systems are expected to collect and process personal data.

7 Conclusion

This paper introduced the SoP architecture and discussed the use of SoPs for wearable computing systems. By combining the advantages of flexible electronics and silicon technology, SoP architectures offer a great potential in transforming wearable computing. However, there are many design and technology challenges in adapting SoP architectures. As the first step in addressing these challenges, we introduced the maximum deflection of a flexible substrate as a new metric, flexibility, in addition to traditional power, area and performance metrics. Using this new metric, we developed a methodology for the optimal placement of rigid chips on flexible substrates to maximize flexibility. The optimal placements shows 5.7× enhancement in flexibility compared to a naïve placement. Finally, we validated the optimization scenarios through FEM simulations, and we presented a SoP prototype targeting sensing applications.

8 Acknowledgments

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Ujjwal Gupta received the B.E. degree from Manipal University, KA, India, in 2011, in Electronics and Communication Engineering, and the M.S. degree from Arizona State University, Tempe, AZ, in 2014, in Electrical Engineering. He is currently working toward the Ph.D. degree in the Department of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ. His research interests are scaling trends in computer architectures, energy optimization in diverse computing platforms, RTL design on FPGAs, and emerging system design methodologies.

Jaehyun Park received the B.S. in Electrical Engineering and Ph.D degree in Electrical Engineering and Computer Science from Seoul National University, Seoul, Korea, in 2006 and 2015, respectively. From 2009 to 2010, he was a Visiting Scholar with the University of Southern California, Los Angeles, CA. He is currently an Exchange Scholar with School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ. His current research interests include flexible hybrid electronics, low-power embedded system design and non-volatile memory system design.

Hitesh Joshi received his B.Tech in Electronics & Instrumentation Engineering from UPTU, Lucknow, India. He is currently pursuing his MS degree in Electrical Engineering from Arizona State University. His specialization is Electronics and Mixed Signal Circuit Design. His research interests are related to Embedded Systems, Flexible Hybrid Electronics (FHE).

Umit Y. Ogras received his Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh, PA, in 2007. From 2008 to 2013, he worked as a Research Scientist at the Strategic CAD Laboratories, Intel Corporation. He is currently an Assistant Professor at the School of Electrical, Computer and Energy Engineering. Recognitions Dr. Ogras has received include Strategic CAD Labs Research Award, 2012 IEEE Donald O. Pederson Transactions on CAD Best Paper Award, 2011 IEEE VLSI Transactions Best Paper Award and 2008 EDAA Outstanding PhD. Dissertation Award. His research interests include digital system design, embedded systems, multicore architecture and electronic design automation with particular emphasis on multiprocessor systems-on-chip (MPSoC).

APPENDIX

In this section, we present the proof of the theorem that specifies the optimal placement along one dimension.

Theorem 1: Consider the placement of N rigid chips along one dimension (e.g., x-axis as shown in Figure 4).

1) *If the rigid chips are **not allowed to overlap**,* the flexibility is maximized when all the chips are placed side by side (i.e., they form a contiguous region), at either side of the substrate, as illustrated in Figure 7. The maximum flexibility in this case is given as,

$$\delta_{\text{nonoverlapping}} = \frac{P_{\max}}{3EI}\left(L - \sum_{i=1}^{N} l_i\right)^3 \tag{7}$$

2) *If the rigid chips **can overlap**,* the flexibility is maximized if the chips are placed at either side, and the overlap between each pair is *maximum*, as illustrated in Figure 7.
The maximum flexibility in this case is given as,

$$\delta_{\text{overlapping}} = \frac{P_{\max}}{3EI}\left(L - \max_{1\le i\le N} l_i\right)^3 \tag{8}$$

Proof of part 1: Consider the flexibility of non-overlapping chips shown in Equation 4,

$$\delta(\boldsymbol{x}) = \frac{P_{\max}}{3EI}\left[x_1^3 + \sum_{i=1}^{N-1}(x_{i+1} - (x_i + l_i))^3 + (L - (x_N + l_N))^3\right]$$

Derivative w.r.t. x_1: The first and second order analytical derivatives of Equation 4 w.r.t. x_1 are:

$$section\frac{\partial\delta(\boldsymbol{x})}{\partial x_1} = \frac{P_{\max}}{3EI}\left[3x_1^2 - 3(x_2 - x_1 - l_1)^2\right] \tag{19}$$

$$\frac{\partial^2\delta(\boldsymbol{x})}{\partial x_1^2} = \frac{P_{\max}}{3EI}\left[6x_1 + 6(x_2 - x_1 - l_1)\right] \tag{20}$$

Since $0 \le x_1 \le x_2 - l_1$, the second order derivative in Equation 20 is non-negative. This implies that the first order derivative $\frac{\partial\delta(\boldsymbol{x})}{\partial x_1}$ is non-decreasing. The first order derivatives at the boundaries of x_1 can be written as,

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_1}\right|_{x_1=0} = \frac{P_{\max}}{3EI}\left[-3(x_2 - l_1)^2\right] \le 0 \tag{21}$$

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_1}\right|_{x_1=x_2-l_1} = \frac{P_{\max}}{3EI}\left[3(x_2 - l_1)^2\right] \ge 0 \tag{22}$$

Equation 21 implies that $\delta(\boldsymbol{x})$ is decreasing or flat at $x_1 = 0$, while Equation 22 implies that $\delta(\boldsymbol{x})$ is increasing or constant at $x_1 = x_2 - l_1$. Since the first order derivative is non-decreasing, the flexibility $\delta(\boldsymbol{x})$ has to be maximum at one of the boundaries $x_1 = 0$ or $x_1 = x_2 - l_1$.

Derivative w.r.t. x_i: The first and second order derivatives w.r.t. $x_i,\ \text{for } 1 < i < N$ can be written as,

$$\frac{\partial\delta(\boldsymbol{x})}{\partial x_i} = \frac{P_{\max}}{3EI}\left[3(x_i - x_{i-1} - l_{i-1})^2 - 3(x_{i+1} - x_i - l_i)^2\right] \tag{23}$$

$$\frac{\partial^2\delta(\boldsymbol{x})}{\partial x_i^2} = \frac{P_{\max}}{3EI}\left[6(x_i - x_{i-1} - l_{i-1}) + 6(x_{i+1} - x_i - l_i)\right] \tag{24}$$

Since $x_{i-1} + l_{i-1} \le x_i \le x_{i+1} - l_i$, the derivative $\frac{\partial^2\delta(\boldsymbol{x})}{\partial x_i^2}$ is non-negative, which implies the first order derivative $\frac{\partial\delta(\boldsymbol{x})}{\partial x_i}$ is non-decreasing. Furthermore, the first order derivative at the lower and higher boundaries of x_i can be written as,

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_i}\right|_{x_i=x_{i-1}+l_{i-1}} = \frac{P_{\max}}{3EI}\left[-3(x_{i+1} - x_{i-1} - l_{i-1} - l_i)^2\right] \le 0 \tag{25}$$

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_i}\right|_{x_i=x_{i+1}-l_i} = \frac{P_{\max}}{3EI}\left[3(x_{i+1} - l_i - x_{i-1} - l_{i-1})^2\right] \ge 0 \tag{26}$$

Again, $\delta(\boldsymbol{x})$ is decreasing or flat at the lower bound, and it is increasing or flat at the upper bound. Since the first order derivative is non-decreasing, the flexibility $\delta(\boldsymbol{x})$ has to be maximum at one of the boundaries.

Derivative w.r.t. x_N: The first and second order derivatives w.r.t. x_N can be written as,

$$\frac{\partial\delta(\boldsymbol{x})}{\partial x_N} = \frac{P_{\max}}{3EI}\left[3(x_N - x_{N-1} - l_{N-1})^2 - 3(L - x_N - l_N)^2\right] \tag{27}$$

$$\frac{\partial^2\delta(\boldsymbol{x})}{\partial x_N^2} = \frac{P_{\max}}{3EI}\left[6(x_N - x_{N-1} - l_{N-1}) + 6(L - x_N - l_N)\right] \tag{28}$$

Since $x_{N-1} + l_{N-1} \le x_N \le L - l_N$, the derivative $\frac{\partial^2\delta(\boldsymbol{x})}{\partial x_N^2}$ is non-negative, which implies the first order derivative $\frac{\partial\delta(\boldsymbol{x})}{\partial x_N}$ is non-decreasing. Furthermore, the first order derivative at the lower and upper bounds of x_N can be written as,

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_N}\right|_{x_N=x_{N-1}+l_{N-1}} = \frac{P_{\max}}{3EI}\left[-3(L - x_{N-1} - l_{N-1} - l_N)^2\right] \le 0 \tag{29}$$

$$\left.\frac{\partial\delta(\boldsymbol{x})}{\partial x_N}\right|_{x_N=L-l_N} = \frac{P_{\max}}{3EI}\left[3(L - l_N - x_{N-1} - l_{N-1})^2\right] \ge 0 \tag{30}$$

By the same token, the flexibility $\delta(\boldsymbol{x})$ has to be maximum at one of the boundaries, $x_N = x_{N-1} + l_{N-1}$ or $x_N = L - l_N$. As a result, the flexibility is maximized when all the chips are placed side by side (i.e., they form a contiguous region), at either side of the substrate.

A particular optimal solution instance is $x_1 = 0$ and $x_i = x_{i-1} + l_{i-1}$ for $2 \le i \le N$. The maximum displacement in this case evaluates to:

$$\delta_{\text{nonoverlapping}} = \frac{P_{\max}}{3EI}\left(L - \sum_{i=1}^{N} l_i\right)^3 \tag{31}$$

QED.

Proof of part 2: Consider the maximum deflection of overlapping chips shown in Equation 6,

$$\delta(x_1, \boldsymbol{o}) = \frac{P_{\max}}{3EI}\left[x_1^3 + \left(L - \left(x_1 + \sum_{i=1}^{N} l_i - \sum_{i=1}^{N-1} o_i\right)\right)^3\right]$$

Derivative w.r.t. x_1**:** The first and second order derivatives of Equation 6 w.r.t. x_1 are:

$$\frac{\partial \delta(x_1, \boldsymbol{o})}{\partial x_1} = \frac{P_{\max}}{3EI}\left[3x_1^2 - 3\left(L - x_1 - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N-1} o_i\right)^2\right] \quad (32)$$

$$\frac{\partial^2 \delta(x_1, \boldsymbol{o})}{\partial x_1^2} = \frac{P_{\max}}{3EI}\left[6x_1 + 6\left(L - x_1 - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N-1} o_i\right)\right] \quad (33)$$

Since $0 \leq x_1 \leq L - l_1$ and the substrate length is large enough to accommodate all the chips, *i.e.*, $L \geq x_1 + \sum_{i=1}^{N} l_i - \sum_{i=1}^{N-1} o_i$, the second order derivative $\frac{\partial^2 \delta(x_1, \boldsymbol{o})}{\partial x_1^2}$ is non-negative. This implies the first order derivative $\frac{\partial \delta(x_1, \boldsymbol{o})}{\partial x_1}$ is either increasing or flat. Furthermore, the first order derivative at the lower and higher boundaries of x_1 can be written as,

$$\left.\frac{\partial \delta(x_1, \boldsymbol{o})}{\partial x_1}\right|_{x_1=0} = \frac{P_{\max}}{3EI}\left[-3\left(L - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N-1} o_i\right)^2\right] \leq 0 \quad (34)$$

$$\left.\frac{\partial \delta(x_1, \boldsymbol{o})}{\partial x_1}\right|_{x_1=L-l_1} = \frac{P_{\max}}{3EI}\left[3(L - l_1)^2 - 3\left(\left(\sum_{i=1}^{N} l_i - \sum_{i=1}^{N-1} o_i\right) - l_1\right)^2\right] \geq 0 \quad (35)$$

At $x_1 = 0$, the first order derivative is negative. At $x_1 = L - l_1$, the first order derivative is positive because $L > \sum_{i=1}^{N} l_i - \sum_{i=1}^{N-1} o_i$. Equation 34 implies that $\delta(x_1, \boldsymbol{o})$ is decreasing or flat at $x_1 = 0$, while Equation 35 implies that $\delta(x_1, \boldsymbol{o})$ is increasing or constant at $x_1 = L - l_1$. Since the first order derivative is non-decreasing, the flexibility $\delta(x_1, \boldsymbol{o})$ has to be maximum at one of the boundaries $x_1 = 0$ or $x_1 = L - l_1$.

Derivative w.r.t. o_i**:** The first order derivative of the Equation 6 w.r.t. the overlap o_i can be written as,

$$\frac{\partial \delta(x_1, \boldsymbol{o})}{\partial o_i} = \frac{P_{\max}}{3EI}\left[3\left(L - x_1 - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N-1} o_i\right)^2\right] \geq 0 \quad (36)$$

Since the first order partial derivative w.r.t. o_i is non-negative, the flexibility $\delta(x_1, \boldsymbol{o})$ is either increasing or flat. Therefore, the maximum value of $\delta(x_1, \boldsymbol{o})$ for a given x_1 occurs, when the overlaps (o_i) are maximum. Since $0 \leq o_i \leq min(l_i, l_{i+1}), \forall\ 1 \leq i < N$, the sum $\sum_{i=1}^{N-1} o_i$ reaches its maximum value when each of the o_i is maximum. As a result, the flexibility is maximized if the chips are placed at either side, and the overlap between each pair is *maximum*.

A particular optimal solution instance is $x_1 = 0$ and $o_i = min(l_i, l_{i+1})$ for $1 \leq l < N$. To plug these values to Equation 6, we need to compute the sum of the overlaps $\sum_i o_i$. We achieve this as follows:

$$\sum_{i=1}^{N-1} \max(o_i) = \sum_{i=1}^{N-1} min(l_i, l_{i+1}) = \sum_{i=1}^{N} l_i - \max_{1 \leq i \leq N} l_i$$

The first equality in this equation follows directly from the upper bound of o_i. The second equality reflects the fact that the summation term $\sum_{i=1}^{N-1} min(l_i, l_{i+1})$ evaluates to the sum of the lengths of all rigid components excluding the length of the longest chip. When we plug the last expression and $x_1 = 0$ to Equation 6, we obtain the maximum flexibility with overlap as:

$$\begin{aligned}
\delta_{\text{overlapping}} &= \frac{P_{\max}}{3EI}\left[L - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N-1} \max(o_i)\right]^3 \\
\delta_{\text{overlapping}} &= \frac{P_{\max}}{3EI}\left[L - \sum_{i=1}^{N} l_i + \sum_{i=1}^{N} l_i - \max_{1 \leq i \leq N} l_i\right]^3 \\
\delta_{\text{overlapping}} &= \frac{P_{\max}}{3EI}\left[L - \max_{1 \leq i \leq N} l_i\right]^3 \quad (37)
\end{aligned}$$

QED.